

1 1. A method of evaluating the performance of a hybrid analog-digital integrated circuit having
2 an analog unit, a digital unit, and a substrate on which the units are located, comprising:
3 identifying a broadband power source that represents noise characteristics of the digital unit;
4 and
5 simulating performance of the integrated circuit by evaluating performance of a lumped circuit
6 in which the source couples to a lumped element representing the substrate and the substrate couples
7 to a lumped element representing the analog unit.

1 2. The method of claim 1, wherein the identifying includes evaluating one or more
2 characteristics of the power source based on a behavioral simulation model for the digital unit.

1 3. The method of claim 1, further comprising:
2 repeating the identifying and simulating for another digital unit; and
3 selecting one of the two digital units based on the simulating showing that the integrated
4 circuit has a better performance with the one of the units.

1 4. The method of claim 1, further comprising:
2 repeating the simulating for a lumped element representing another substrate; and
3 selecting a better one of the two substrates based on the performances determined by the acts
4 of simulating.

1 5. A program storage medium encoding a computer executable program of instructions for
2 evaluating the performance of a hybrid analog-digital integrated circuit having an analog unit, a digital
3 unit, and a substrate on which the units are located, the instructions to cause the computer to:
4 identify a broadband power source that represents noise characteristics of the digital unit; and
5 simulate performance of the integrated circuit by evaluating performance of a lumped circuit
6 in which the source couples to a lumped element representing the substrate and the substrate couples
7 to a lumped element representing the analog unit.

1 6. The medium of claim 5, wherein the instruction to identify evaluates one or more
2 characteristics of the power source based on a behavioral simulation model for the digital unit.

1 7. The medium of claim 5, wherein the instructions further cause the computer to:
2 repeat the identifying and simulating for another digital unit; and
3 select one of the two digital units based on the simulating showing that the integrated
4 circuit has a better performance with the one of the units.

1 8. The medium of claim 5, wherein the instructions further cause the computer to:
2 repeat the simulating for a lumped element representing another substrate; and
3 select a better one of the two substrates based on the performances determined by the
4 acts of simulating.

1 9. A method comprising:
2 identifying a candidate integrated circuit that comprises a candidate digital circuit;
3 determining a power coefficient, S_0 , of said candidate digital circuit;
4 predicting a power spectral density, $S(\omega)$, of said candidate digital circuit based on said
5 power coefficient, S_0 , of said candidate digital circuit; and
6 fabricating said candidate integrated circuit when said power spectral density, $S(\omega)$, of said
7 candidate digital circuit achieves a design goal for said candidate integrated circuit.

1 10. The method of claim 9 further comprising determining a mean bit rate, \bar{v} , of said
2 candidate digital circuit, wherein said power spectral density, $S(\omega)$, of said candidate digital circuit is
3 based on said power coefficient, S_0 , and on said mean bit rate, \bar{v} .

1 11. The method of claim 9 wherein said candidate integrated circuit further comprises a
2 candidate analog circuit.

1 12. The method of claim 11 further comprising evaluating a lumped circuit in which a noise
2 source based on $S(\omega)$ is coupled to a multi-port network that represents a candidate substrate which is
3 coupled to a multi-port network that represents said candidate analog circuit.

1 13. The method of claim 9 wherein said candidate integrated circuit comprises a plurality of
2 candidate digital circuits.

1 14. The method of claim 9 wherein said power coefficient, S_0 , is based on the number of
2 switching devices composing said candidate digital circuit.

1 15. The method of claim 9 wherein said power coefficient, S_0 , is based on the clock rate of
2 said candidate digital circuit.

1 16. The method of claim 9 wherein said power coefficient, S_0 , is based on a plurality of
2 voltage levels of said candidate digital circuit.

1 17. The method of claim 9 wherein said power coefficient, S_o , is based on an activity factor of
2 said candidate digital circuit.

3 18. A method comprising:
4 identifying a candidate integrated circuit that comprises a candidate digital circuit;
5 determining a mean bit rate, $\bar{\nu}$, of said candidate digital circuit;
6 predicting a power spectral density, $S(\omega)$, of said candidate digital circuit based on said mean
7 bit rate, $\bar{\nu}$, of said candidate digital circuit; and
8 fabricating said candidate integrated circuit when said power spectral density, $S(\omega)$, of said
9 candidate digital circuit achieves a design goal for said candidate integrated circuit.

1 19. The method of claim 18 further comprising determining a power coefficient, S_o , of said
2 candidate digital circuit, wherein said power spectral density, $S(\omega)$, of said candidate digital circuit is
3 based on said power coefficient, S_o , and on said mean bit rate, $\bar{\nu}$.

1 20. The method of claim 18 wherein said candidate integrated circuit further comprises a
2 candidate analog circuit.

1 21. The method of claim 20 further comprising evaluating a lumped circuit in which a noise
2 source based on $S(\omega)$ is coupled to a multi-port network that represents a candidate substrate which is
3 coupled to a multi-port network that represents said candidate analog circuit.

1 22. The method of claim 18 wherein said candidate integrated circuit comprises a plurality of
2 candidate digital circuits.

1 23. The method of claim 18 wherein said mean bit rate, $\bar{\nu}$, is based on the number of
2 switching devices composing said candidate digital circuit.

1 24. The method of claim 18 wherein said mean bit rate, $\bar{\nu}$, is based on the clock rate of said
2 candidate digital circuit.

1 25. The method of claim 18, wherein said mean bit rate, $\bar{\nu}$, is based on a plurality of voltage
2 levels of said candidate digital circuit.

- 1 **26.** The method of claim 18 wherein said mean bit rate, \bar{v} , is based on an activity factor of
- 2 said candidate digital circuit.

2025 RELEASE UNDER E.O. 14176